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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Joseph A Walkowski
Trask Britt & Rossa
P O Box 2550
Salt Lake City, UT 84110

EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/538,684	KINSMAN ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12,14-20,22-29,33-37 and 39-45* is/are pending in the application.

4a) Of the above claim(s) *7,21,23 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-12,14-20,22,24-29,31,33-37 and 39-45* is/are rejected.

7)☒ Claim(s) *1-4,6,8-12,14-20,22,24-29,31,33-37 and 39-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim 1: "the plurality of leads having portions enclosed within the package body forming an area"; "the plurality of leads having a reduced lead inductance"; "a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body"; "the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries";

Claim 10: "wherein the second portion of the heat sink projects substantially to" "a top" "of the package body";

Claim 22: "the plurality of leads having reduced lead inductance"; the plurality of leads having portions enclosed within the package body forming an area"; "a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame

having portions enclosed within the package body forming an area"; "reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries";

Claim 24: "the plurality of leads having a reduced lead inductance"; "the plurality of leads having portions enclosed within the package body forming an area"; "extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body"; "reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries";

Claim 25: "a plurality of leads having a reduced lead inductance"; "the plurality of leads forming an area"; "a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame"; "the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries";

Claim 34: "wherein the second portion of the heat sink projects substantially to" "a top" "of the package body" ; and,

The entirety of claims 16 and 41.

The following is a quotation of 37 CFR 1.84 Standards for drawings:

(p) Numbers, letters, and reference characters.
(1) Reference characters (numerals are preferred), sheet numbers, and view numbers must be plain and legible, and must not be used in association with brackets or inverted commas, or enclosed within outlines, e.g., encircled. They must be oriented in the same direction as the view so as to avoid having to rotate the sheet. Reference characters should be arranged to follow the profile of the object depicted.
(2) The English alphabet must be used for letters, except where another alphabet is customarily used, such as the Greek alphabet to indicate angles, wavelengths, and mathematical formulas.
(3) Numbers, letters, and reference characters must measure at least.32 cm. (1/8 inch) in height. They should not be placed in the drawing so as to interfere with its comprehension. Therefore, they should not cross or mingle with the lines. They should not be placed upon hatched or shaded surfaces. When necessary, such as indicating a surface or cross section, a reference character may be underlined and a blank space may be left in the hatching or shading where the character occurs so that it appears distinct.
(4) The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.
(5) Reference characters not mentioned in the description shall not appear in the drawings. Reference characters mentioned in the description must appear in the drawings.
(q) Lead lines . Lead lines are those lines between the reference characters and the details referred to. Such lines may be straight or curved and should be as short as possible. They must originate in the immediate proximity of the reference character and extend to the feature indicated. Lead lines must not cross each other. Lead lines are required for each reference character except for those which indicate the surface or cross section on which they are placed. Such a reference character must be underlined to make it clear that a lead line has not been left out by mistake. Lead lines must be executed in the same way as lines in the drawing. See paragraph (l) of this section.
(r) Arrows . Arrows may be used at the ends of lines, provided that their meaning is clear, as follows:
(1) On a lead line, a freestanding arrow to indicate the entire section towards which it points;
(2) On a lead line, an arrow touching a line to indicate the surface shown by the line looking along the direction of the arrow; or
(3) To show the direction of movement.

The drawings are objected to because in Figures 1A, 1B and 1C reference characters 26, 30, 32, 56, 60, 62, 86, 90 and 92 are used in association with brackets.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31-37 and 39-45 are objected to because of the following informalities: The term "nanoheneries" appears to be a misspelling. Appropriate correction is required.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hernandez (4994936).

In the abstract and column 1, lines 6-12; 22-56; column 2, lines 4-17, and 21-64; column 3, line 62 to column 4, line 23; column 4, line 49 to column 5, line 42; column 5, line 55 to column 6, line 2; and column 6, line 35 to column 7, line 61, Hernandez discloses the following:
An integrated circuit package having a plurality of leads and a heat sink, the plurality of leads having reduced lead inductance from that of a conventional electrically isolated heat sink comprising: a package body 27; an integrated circuit die 28 positioned within the package body; a lead frame 10 including a plurality of leads 16 having portions enclosed within the package body that connect to the integrated circuit die (via 30, 32), the plurality of leads having portions enclosed within the package body forming an area; and an

electrically conductive heat sink 60, 68 (and optionally any "molding" directly between 60' and 68) positioned at least partially within the package body with a surface of a first portion 60 (portion of 60 from 66 to distance equal to thickness of 70), 70 of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body "the size of the capacitor is only limited by the distance between the dam bars 18 of the lead frame" and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame inherently at least about 0.90 nanoheneries; wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body; wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory

integrated circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and an inherent processor integrated circuit die; wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame; wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection; wherein the heat sink is positioned only partially within the package body "said stem terminates at a surface which is exterior of said molding material"; wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame; wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body; wherein the first and second portions of the heat sink are integral with one another; wherein the first and second portions of the heat sink comprise separate parts; wherein the heat sink comprises a plurality of parts 60, 70, each forming a portion of both the first and second portions of the heat sink; wherein the heat sink has locking holes 74, 78, 84 therein for locking the heat sink in the integrated circuit package; further comprising an adhesive attaching the lead frame to the heat sink; wherein the integrated circuit package comprises one of a Vertical Surface Mount Package, a Small Outline

J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Package.

An integrated circuit package having a plurality of leads and a heat sink, the plurality of leads having a reduced lead inductance comprising: a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion 60' surrounded by a horizontally extending skirt portion 34 having a vertical thickness, said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

An integrated circuit package having heat sink and a plurality of leads having a reduced lead inductance comprising: an integrated circuit die; a lead frame including a plurality of leads having portions that are connected to the integrated circuit die, the plurality of leads forming an area; and an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries; a package body; wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body; wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated circuit die, a flash

Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die; wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame; wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection; wherein the heat sink is positioned only partially within the package body; wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame; wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body; wherein the first and second portions of the heat sink are integral with one another; wherein the first and second portions of the heat sink comprise separate parts; wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink;, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located; wherein the heat sink has locking holes therein for locking the heat sink in the integrated circuit package; further comprising an adhesive attaching the lead frame to the heat sink; wherein the integrated circuit package comprises one of a Vertical Surface Mount

Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Pack.

To further clarify the disclosure of the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame inherently at least about 0.90 nanoheneries, in the instant specification, paragraphs 32 and 33, applicant discloses that the particular claimed inductance is an inherent result of the process of using the claimed package: "The first portion 26 of the heat sink 28 extends beneath a substantial part of enclosed portions 32 of the leads 16 of the lead frame 18 in close proximity to the leads 16 but separated therefrom by an adhesive insulative layer 38, such as an adhesive tape or screen printed adhesive on the lead frame 18 or the heat sink 28. By extending in such close proximity to the leads 16, the first portion 26 of the heat sink 28 magnetically couples to the leads 16 and reduces the mutual and self inductance associated with the leads 16 as described above. A first portion 26 that extends beneath a 'substantial part' of the enclosed portions 32 of the leads 16 includes, but is not limited to, those first portions that extend beneath substantially all of the enclosed portions of the leads 16, that extend substantially to sides 33 of the IC package 10 as shown in FIG. 1A, and that, for example, extend

beneath at least about eighty percent (80%) of the area of the enclosed portions of the lead frame 18." "Such results have also shown that in another IC package in which the heat sink of the present invention is connected to a signal voltage, lead inductance is reduced from that of a conventional heat sink connected to a signal voltage by about 25 percent (from about 4.60 nH to about 3.47 nH)." Furthermore, as elucidated supra, Hernandez discloses a process of using the package with the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame. Therefore, in the process of using the package of Hernandez, inductance of the plurality of leads of the lead frame is inherently at least about 0.90 nanoheneries.

To further clarify, Hernandez discloses an inherent processor integrated circuit die because Hernandez discloses the following processor integrated circuit die functions: "It is well known in the field of microelectronics that high frequency operation, particularly the switching of integrated circuits, can result in transient energy being coupled into the power supply circuit. It is also well known that integrated circuits are becoming more dense (more gates per unit area of silicon/or gallium arsenide), more powerful (more watts per unit area of IC chip), and faster

with higher clock rate frequencies and with smaller rise times. All of these recent and continued developments make the problem of suppressing noise in the power bus (produced by a large amount of simultaneous gates switching) even more serious than in the past."

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the alternative, claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31-37 and 39-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez (4994936).

Hernandez is applied as it is applied to claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31-37 and 39-45 supra.

However, Hernandez does not appear to explicitly disclose reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

Notwithstanding, Hernandez discloses that lead inductance is a result-effective variable. Moreover, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed lead inductance in the process of using the package because applicant has not disclosed that, in view of the applied prior art, the particular inductance is for a particular **unobvious** purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another process. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the

general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

In the alternative, claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 supra, and further in combination with Wark (5696031).

Hernandez does not appear to disclose literally a "processor."

Still, at column 2, lines 47-63; column 3, lines 9-11; and column 5, lines 59-65, Wark discloses a "processor." In addition, it would have been obvious to combine this disclosure of Wark with the disclosure of Hernandez because it would facilitate provision of the device of Hernandez.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Inasaka (5136471).

As cited, Hernandez discloses wherein a heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage; wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

However, Hernandez does not appear to explicitly disclose wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage.

Nevertheless, as cited, Hernandez discloses wherein a heat sink 34 is coupled by leads 16 to a "circuit board" outside the package body thereby coupled to one of a signal voltage and a reference voltage. Further, at column 2, lines 53-68; and column 4, lines 17-30, Inasaka discloses wherein a package body 30 is coupled to a "printed circuit board" outside the

package body thereby coupled to one of a "signal voltage" and a "reference voltage." Moreover, it would have been obvious to combine these disclosures of the applied prior art because it would facilitate provision of the circuit board, signal voltage and reference voltage of the embodiment of Hernandez applied to claim 1.

In the alternative, claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Inasaka as applied to claims 9 and 10 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Nakamura (JP5102338).

Hernandez does not appear to explicitly disclose wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

Regardless, in the English abstracts and Figure 3, Nakamura discloses wherein the surface of the first portion of the heat sink 1 includes a recess 7 in which the die-attach area is located. Furthermore, it would have been obvious to combine this disclosure of Nakamura with the disclosure of Hernandez because it would facilitate the heat transmission of Hernandez, enable die alignment and adhesive containment, and as disclosed by

Inasaka, it would hold the die, reduce mounting height, increase mounting density, enable plating bar cutting and reduce cost.

In the alternative, claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Nakamura as applied to claim 17 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Wark (5696031).

As cited, Hernandez discloses an integrated circuit package having a plurality of leads and a heat sink, the plurality of leads having reduced lead inductance comprising a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body forming an area and having a die-attach area on the surface

of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink and the integrated circuit die for reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

However, Hernandez does not appear to explicitly disclose an electronic system having an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices.

Nevertheless, as cited supra, Wark teaches these limitations. Moreover, it would have been obvious to combine this disclosure of Wark with the disclosure of Hernandez because it provide low inductance devices in the system of Wark, and facilitate provision of the device of Hernandez.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 26, and further in combination with Inasaka (5136471).

As cited, Hernandez discloses wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame; wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

However, Hernandez does not appear to explicitly disclose wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage.

Nevertheless, as cited, Hernandez discloses wherein a heat sink 34 is coupled by leads 16 to a "circuit board" outside the package body thereby coupled to one of a signal voltage and a reference voltage. Further, at column 2, lines 53-68; and column 4, lines 17-30, Inasaka discloses wherein a package body 30 is coupled to a "printed circuit board" outside the package body thereby coupled to one of a "signal voltage" and a "reference voltage." Moreover, it would have been obvious to combine these disclosures of the applied prior art because it would facilitate provision of the circuit board, signal voltage and reference voltage of the embodiment of Hernandez applied to claim 26.

In the alternative, claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Inasaka as applied to claim 34 and 35 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra.

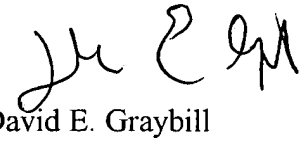
Applicant's remarks filed 11-28-6 have been fully considered and are moot in view are the new grounds of rejection.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.



David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
14-Mar-07

In view of the appeal brief filed on 11-28-6, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Zandra V Smith

Zandra V. Smith
Supervisory Patent Examiner

16 March 2007